UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,819	01/16/2004	Douglas Todd Hayden	10002614-1	7995

22879 7590 08/04/2010

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS, CO 80528

EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
08/04/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
ipa.mail@hp.com
laura.m.clark@hp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DOUGLAS TODD HAYDEN

Appeal 2008-005639
Application 10/759,819
Technology Center 2100

Before JOHN A. JEFFERY, LANCE LEONARD BARRY, and ST. JOHN COURTENAY III, *Administrative Patent Judges.*

BARRY, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

---

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-7, 9-11, and 31-36. The Appellant appeals therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

INVENTION

The Appellant describes the invention at issue on appeal as follows.

> [T]he system comprises a bus comprising signal lines and a device configured to be inserted onto and removed from the bus through contacts. The contacts are configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit.

(Spec. 22.)

ILLUSTRATIVE CLAIM

1. A system comprising:

a bus comprising signal lines; and

a device configured to be inserted onto and removed from the bus through contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit.

REJECTIONS

Claims 1-6, 9, 10, 31-33, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,729,062 (Satoh).

Claim 7 stands rejected under § 103(a) as being unpatentable over Satoh and Li (Paul Li, *LVTC Logic Family for Live-Insertion Using Standard CMOS Process*, 1-3 (Pericom Semiconductor Corp., Jan. 24, 2003, *available at* http://www.pericom.com/pdf/ applications/AN062.pdf (hereinafter "Li")) .

Claim 11 stands rejected under § 103(a) as being unpatentable over Satoh and The I^2C-Bus Specification (Philips Semiconductors: The I^2C-Bus Specification, Version 2.1 Jan. 2000, *available at* http://www.nxp.com/ acrobat_download2/literature/ 9398/39340011.pdf).

Claims 34 and 36 stand rejected under § 103(a) as being unpatentable over Satoh and U.S. Patent No. 5,644,731 (Liencres).

CLAIMS 1-7 AND 9-11

Based on the Appellant's arguments, we will decide the appeal of claims 1-7 and 9-11 based on claim 1 alone. Regarding this claim, the Examiner makes the following findings and conclusions.

> [O]ne of ordinary skill in the art at the time the invention was made would have found it obvious to incorporate the teaching of Fig. 9 into Fig. 5 (achieving illustrative drawing Fig. 5 in view of Fig. 9 above) such that the use of pre-charge circuit 18a_50 (or 18b_50) "limits a rush to flow when the" bus signal "is connected to the terminal of the mother board connector" (Satoh; col. 6, ll.18-20) . . . . The combination of Fig. 5 in view of Fig. 9 . . . clearly shows the pre-charge circuit contact 18a_57 makes contact with the motherboard connector prior to signal line contact 18a_59 based on the length of the contacts.

(Ans. 15.) The Appellant argues that "the Examiner is using the novel elements of the independent claims as an instruction set or recipe to build a

circuit and then inserting (without suggestion from Satoh itself) the circuit into Satoh's figures." (Reply Br. 2.) He further argues that Figure 5 of Satoh "does not suggest a pre-charge circuit. Satoh never suggests a signal line and pre-charge circuit to engage at different times." (*Id.* at 3.) The Appellant also argues that "[n]o suggestion whatsoever exists in Satoh for providing a low-impedance across a pre-charge circuit." (*Id.* at 2.)

Therefore, the *issue* before us is whether the Examiner erred in combining teachings from Figures 5 and 9 of Satoh and in finding that those combined teachings would have suggested a pre-charge circuit, a low-impedance across the pre-charge circuit, and a signal line and pre-charge circuit to engage at different times.

FINDINGS OF FACT

Satoh discloses the following invention.

> [A]n active plug-in circuit for allowing a package to be plugged in an active apparatus has a mode setting section for setting either a plug-in mode or a regular mode, depending on the power source voltage of the package. A power consumption controller maintains an electronic circuit built in the package in a low power consumption mode when the mode setting section sets the plug-in mode. A resistor is connected between a power source pin of a connector of the package and a power source terminal of the electronic circuit. A switch short-circuits the resistor when the mode setting section sets the regular mode.

(Col. 1, ll. 30-41.) The reference's "FIG. 5 shows a specific arrangement for setting up the low power consumption mode in [an] electronic circuit 14." (Col. 4, ll. 38-39.) Satoh's "FIG. 9 . . . describ[es] a further alternative embodiment of the present invention." (Col. 5, ll. 62-64.)

ANALYSIS

The presence or absence of a reason "to combine references in an obviousness determination is a pure question of fact." *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). "Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness." *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009). A reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Here, the embodiments from which the Examiner proposes to combine teachings are shown in Figures 5 and 9 of Satoh. Because these two embodiments are disclosed in the same patent, combining them does not require "a leap of inventiveness." *Boston Scientific Scimed.*, 554 F.3d at 991. Furthermore, the embodiment of Figure 9 features "[t]he resistor 50 [that] limits a rush current to flow when the power source pin 57 of the package connector is connected to the terminal of the mother board connector 64." (Col. 6, ll. 18-21.) "In the plug-in mode, i.e., until the regular mode signal appears on the mode signal line 51, the power consumption controller 53 maintains the electronic circuit 52 in the low power consumption mode." (*Id.* at ll. 21-24.) We agree with the Examiner's finding that such an advantage would have given those skilled in the art reason to combine this teaching with those of Figure 5.

"The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art." *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *Keller*, 642 F.2d at 425). In determining obviousness, furthermore, a reference "must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole." *Id.*

Here, we agree with the Examiner that the combination of teachings from Figures 5 and 9 of Satoh would have resulted in the following circuitry.

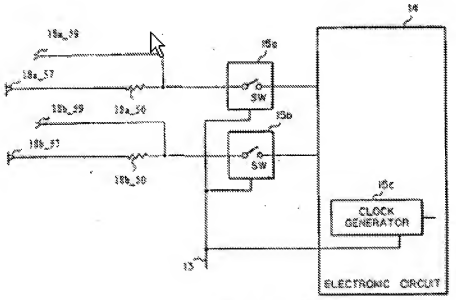

Fig. 5 in view of Fig. 9

(Ans. 6.) As mentioned *supra*, the Examiner finds that this combination circuitry would have suggested a pre-charge circuit 18a_50 or 18b_50. For his part, the Appellant merely argues that Figure 6 individually does not

disclose the pre-charge circuit. Such an individual attack on one embodiment of the reference cannot establish non-obviousness.

"The Examiner has the initial burden to set forth the basis for any rejection so as to put the patent applicant on notice of the reasons why the applicant is not entitled to a patent on the claim scope that he seeks - the so [-]called '*prima facie case*.'" *Ex parte Frye*, No. 2009-006013, 2010 WL 889747, at *3 (BPAI Feb. 26, 2010) (precedential) (citations omitted). "'On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.'" *In re Kahn*, 441 F.3d 977, 985-86 (Fed.Cir. 2006) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed.Cir. 1998)). "[T]he Board reviews the particular finding(s) contested by an appellant anew in light of all the evidence and argument on that issue." *Frye*, 2010 WL 889747 at *4. "Filing a Board appeal does not, unto itself, entitle an appellant to *de novo* review of all aspects of a rejection. If an appellant fails to present arguments on a particular issue - or, more broadly, on a particular rejection - the Board will not, as a general matter, unilaterally review those uncontested aspects of the rejection." *Id.* (citations omitted). "It is not the function of [the U.S. Court of Appeals for the Federal Circuit] to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art." *In re Baxter Travenol Labs.,* 952 F.2d 388, 391 (Fed. Cir. 1991). "Similarly, it is not the function of this Board to examine claims in greater detail than argued by an appellant, looking for distinctions over the prior art." *Ex Parte Shen*, No. 2008-0418, 2008 WL 4105791 at * 9 (BPAI 2008).

Here, the Examiner finds that the aforementioned combination circuitry would have suggested that "signal contact line 18a_59, representing the low-impedance path, is provided across the pre-charge circuit when the contact 18a_59 mates with the motherboard connector" (Ans. 15) and that "the pre-charge circuit contact 18a_57 makes contact with the motherboard connector prior to signal line contact 18a_59 based on the length of the contacts." (*Id.*) For his part, the Appellant summarily alleges that Satoh does not suggest such limitations. (Reply Br. 2.) He does not address, however, let alone show error in, the Examiner's specific findings. We reviewed the particular findings contested by the Appellant in light of his allegations. We refused, however, to examine claim 1 in greater detail than argued by the Appellant, looking for distinctions over the prior art.

Based on the aforementioned facts and analysis, we *conclude* that the Examiner did not err in combining teachings from Figures 5 and 9 of Satoh and in finding that those combined teachings would have suggested a pre-charge circuit, a low-impedance across the pre-charge circuit, and a signal line and pre-charge circuit to engage at different times.

CLAIMS 31-36

Based on the Appellant's arguments, we will decide the appeal of claims 31-36 based on claim 31 alone. The Examiner finds that the aforementioned combination circuitry would have suggested the limitations of claim 31. Besides repeating the unpersuasive arguments made for claim 1, the Appellant asks "where does Satoh teach or suggest two connectors where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line"

(App. Br. 8), and "[w]here is a second conductor that provides a short-circuit between itself and a bus line?" (*Id.*) He argues that "[these] arrangement[s] simply do[ ] not exist in Fig. 9." (*Id.*) The Appellant also argues that "Satoh is directed to power supply contacts and reducing the variation of a power source current occurring when the power source pin of a package connector is connected to the corresponding terminal of a mother board connector and during the transition from a plug-in mode to a regular mode." (*Id.* at 8-9.)

Therefore, the *issue* before us is whether the Examiner erred in finding that the combined teachings from Figures 5 and 9 of Satoh would have suggested a connector system including a first and second connector, where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line, and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system.

ANALYSIS

The Examiner finds that the combination circuitry would have suggested the following limitations:

> a connector system including a first connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_57; please see rejection of claim 1 above), a second connector (Illustrative drawing Fig. 5 in view of Fig. 9 above 18a_59; please see rejection of claim 1 above), where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system (col. 5, line 62 -col. 6, line 27; please see rejection of claim 1 above).

(Ans. 9.)

For his part, the Appellant merely argues that Figure 9 individually does not disclose two connectors where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line and the second conductor that provides a short-circuit between itself and a bus line. (App. Br. 8.) Such an individual attack on one embodiment of the reference cannot establish non-obviousness.

Regarding the staggered connectors, the Appellant merely summarizes Satoh. (*Id.* at 8-9.) He does not address, however, let alone show error in, the Examiner's specific findings. We reviewed the particular findings contested by the Appellant in light of his allegations. We refused, however, to examine claim 31 in greater detail than argued by the Appellant, looking for distinctions over the prior art.

Based on the aforementioned facts and analysis, we *conclude* that the Examiner did not err in finding that the combined teachings from Figures 5 and 9 of Satoh would have suggested a connector system including a first and second connector, where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line, and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system.

DECISION

We affirm the rejections of claims 1-7, 9-11, and 31-36.

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

llw

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS CO 80528